## Overview

The EtherStem module is one of a family of 40-pin BrainStem modules which share a common IO interface meant for docking to breakout boards, prototyping boards and OEM solutions on a 0.1 inch [0.254 mm] spaced header. The only difference in functionality and form-factor is the link transport which through an Ethernet connection.

## Features

- 3 Analog (ADC) Inputs at 12-bit resolution
- ADC sampling up to 200kS/s
- ADC bulk capture to RAM up to 3kS
- 15 GPIO Digital Input/Outputs (3.3 V)
- 1 DAC, 10-bit resolution
- $I^2C$ Fast Mode Plus (Fm+, 1Mbit) intended for BrainStem bus
- $I^2C$ Fast Mode (Fm, 400kbit) user peripheral applications
- User, Link status, Power, Heartbeat LEDs
- 2 Serial Ports (UARTs) with TX and RX Traffic Indication
- 48kB persistent internal storage (4kB slots)
- 1 Internal 8kB RAM Storage Slot
- $\mu$SD Card Interface (max 255 slots of 64kB slots)
- Small size footprint (50.8 mm x 30.48 mm x 14.03 mm)

## Applications

The BrainStem EtherStem Module is a modular power supply subsystem designed for supplying software controllable voltage power rail to a device under test (DUT) in automated testing environments and research and development. Accurate voltage, temperature and current rail measurements can be read through the BrainStem API.

## Description

The BrainStem EtherStem Module is a core BrainStem microcontroller module intended for general purpose applications. The BrainStem EtherStem Module can be easily integrated into any system in order to provide a collection of IO functions for automation systems, embedded control systems and remote data collection. It supports GPIO, I2C, A2D, and DAC. The module provides a flexible embedded virtual machine runtime with simple programming interface to enable use with a wide range of input and output devices. There is also a powerful host-side C/C++ API which enables host-PC interactions with the module and subordinate hardware devices. All Acroname software and APIs are full featured on all host platforms (Mac, Windows, Linux).

## Absolute Maximum Ratings

Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute-maximum-rated conditions for extended periods affects device reliability.

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Input Voltage (Vsupply) | | -0.5 | - | 4.6 | V |
| Supply Current (per pin) | | 0.0 | - | 100.0 | mA |
| Ground Current (per pin) | | 0.0 | - | 100.0 | mA |
| Input Voltage (all pins) | | -0.5 | - | 4.6 | V |
| Operating Temperature | | 0.0 | 25.0 | 80.0 | C |

## Recommended Operating Ratings

The values presented apply over the full operating temperature, otherwise specifications are at $T_A$ = 25 °C.

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Input Voltage (VCC) | | 2.4 | 3.3 | 3.6 | V |
| RTC Supply Voltage (VRTC) | | 2.1 | 3.3 | 3.6 | V |
| Nominal Supply Current | Operating at 25C with 3.3V input voltage | - | 72.2 | - | mA |
| Supply Current (Deep sleep) | Operating at 25C with 3.3V input voltage | - | 180.0 | - | uA |
| ADC Maximum Input Voltage | | -0.5 | - | 4.6 | V |
| ADC Usable Input Voltage Range | | 0.0 | - | 3.3 | V |
| DAC Voltage Output | | 0.0 | - | 3.3 | V |
| Digital Input Voltage | | 0.0 | - | 5.5 | V |
| GPIO Current, per pin | | 18.0 | 20.0 | 22.0 | mA |
| GPIO Input Logic Low Threshold | | - | - | 1.0 | V |
| GPIO Input Logic High Threshold | | 2.3 | - | - | V |
| GPIO Output Voltage | | 0.0 | - | 3.3 | V |
| Operating Temperature | | 0.0 | - | 80.0 | C |
| Unregulated Voltage Input Measurement | | 0.0 | - | 32.76 | V |

## Block Diagram

The BrainStem EtherStem Module is composed of a many different subsystems carefully linked together.

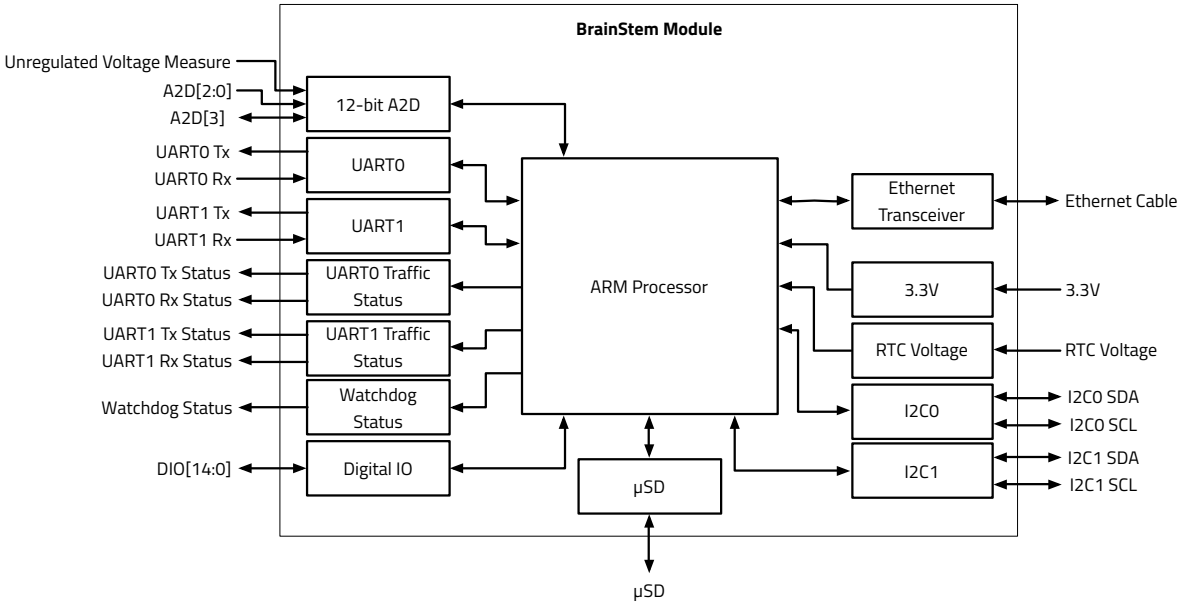


Figure 1: System block diagram

## Pin Functionality

All pin mapping functionality is described in the following table.

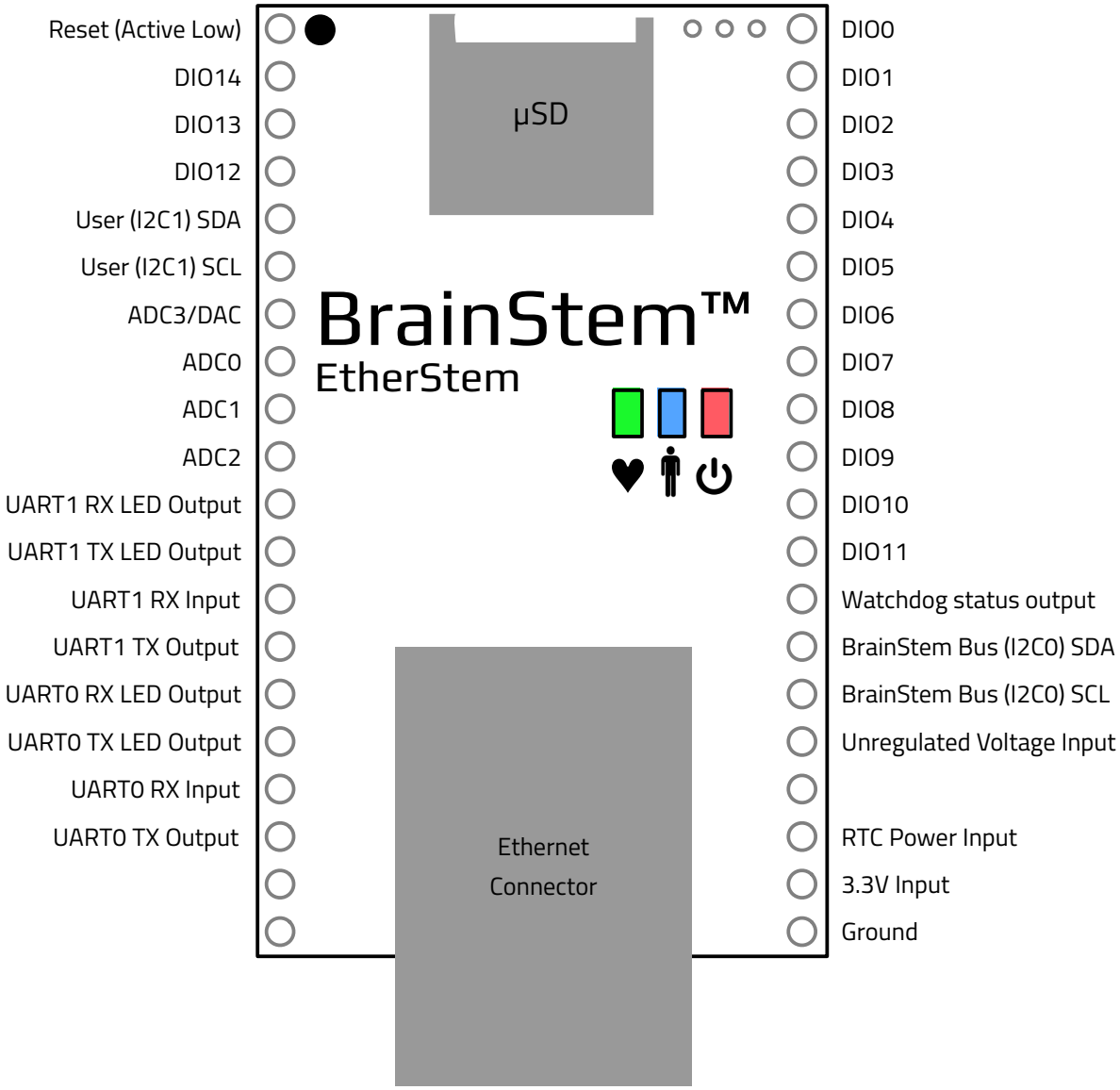


Figure 2: BrainStem EtherStem Module pinout drawing.

| Connector | Description | Notes |
|---|---|---|
| 1 | Reset | Logic low asserts reset |
| 2 | DIO 14 | |
| 3 | DIO 13 | |
| 4 | DIO 12 | |
| 5 | I2C1 SDA | Hardware pull up is included |
| 6 | I2C1 SCL | Hardware pull up is included |
| 7 | ADC3/DAC | Analog input and output capable |
| 8 | ADC0 | Analog input only |
| 9 | ADC1 | Analog input only |
| 10 | ADC2 | Analog input only |
| 11 | UART1 Rx LED status indication | |
| 12 | UART1 Tx LED status indication | |
| 13 | UART1 Rx | |
| 14 | UART1 Tx | |
| 15 | UART0 Rx LED status indication | |
| 16 | UART0 Tx LED status indication | |
| 17 | UART0 Rx | |
| 18 | UART0 Tx | |
| 19 | USB D+ passthrough | |
| 20 | USB D- passthrough | |
| 21 | Ground | |
| 22 | VCC | Recommended 3.3V. See electrical characteristics |
| 23 | RTC Voltage input | Recommended 3.3V. See electrical characteristics |
| 24 | Voltage Transport | 5.0V from USB VBUS is passed through from mini-b connector. |
| 25 | Voltage Unregulated Measure | |
| 26 | I2C0 SCL | Hardware pull up is included. This is primarily used as BrainStem network bus. |
| 27 | I2C0 SDA | Hardware pull up is included. This is primarily used as BrainStem network bus. |
| 28 | Watchdog status pin | |
| 29 | DIO 11 | |
| 30 | DIO 10 | |
| 31 | DIO 9 | |
| 32 | DIO 8 | |
| 33 | DIO 7 | |
| 34 | DIO 6 | |
| 35 | DIO 5 | |
| 36 | DIO 4 | |
| 37 | DIO 3 | |
| 38 | DIO 2 | |
| 39 | DIO 1 | |
| 40 | DIO 0 | |

# Operation

## I2C Interface

The modules supports I2C communication up to fast-mode plus (Fm+, 1MHz). This I2C bus is normally dedicated to communication between other BrainStem and BrainStem Spindle modules, but may also be used for user specific applications. The I2C interface allows the module to operate as a master or slave on the bus, and can support multi-master busses. 330Ωpull-up resistors to 3.3V are incorporated into the module. SCL and SDA lines are 5.0V tolerant.

## Module Power

Regulated 3.3V is required to run the BrainStem EtherStem Module . When all GPIO and analog functions are disabled (default configuration), the module draws the nominal current defined in the ratings table. Current from enabling these functions is additive to the nominal current and the supply should be capable of sourcing the required current without dropping below the minimum input voltage.

Note that the module is not directly powered from the USB 5V VBUS. An unregulated voltage output pin passes the USB VBUS power allowing a subordinate board to regulate and provide the required 3.3V for the module.

Alternatively, 3.3V power may be generated from a source independent from the USB connection, such as a battery. Note that direct connection to standard lithium polymer (LiPo) or lithium ion (LIB) battery voltages will likely allow the module to power on. However, these voltages exceed the recommended input voltage range and doing so voids the warranty.

A measurement of the unregulated system input voltage is available through the programming interface. Measurement granularity is approximately 8mV across the specified input range. It is recommended to have a minimum of 1nF of capacitance on the unregulated voltage measurement to reduce noise on this measurement.

## LED Indicators

The core module has a bank of four LED indicators with specific utility.

| Color | Name | Description |
|---|---|---|
| Yellow | Link LED | Shows the module has established communication with a host processor. Drivers will need to be installed for the BrainStem EtherStem Module for this to happen. Drivers are available through the Acroname Download Center. |
| Green | Heartbeat LED | Cycles on and off when a host application is communicating with the module. |
| Blue | User LED | User application controllable LED. Please see the BrainStem Reference manual for programming interfacing details. |
| Red | Power LED | Shows the core module is receiving 3.3 V power. See the section on Input Power for more details. |

## Power Saving Modes

Significant power consumption reduction can be realized by operating in a low power mode. Using power-saving mode put the microcontroller into a deep sleep state while maintaining the real time clock. The real time clock may be powered by an independent power source through the interface header, such as a standard coin-cell battery. When a single power source is used, it is recommended to tie the RTC Voltage input pin to the 3.3 V input power. Leaving the RTC Voltage pin unconnected will disable the use of any power savings modes.

## Mechanical

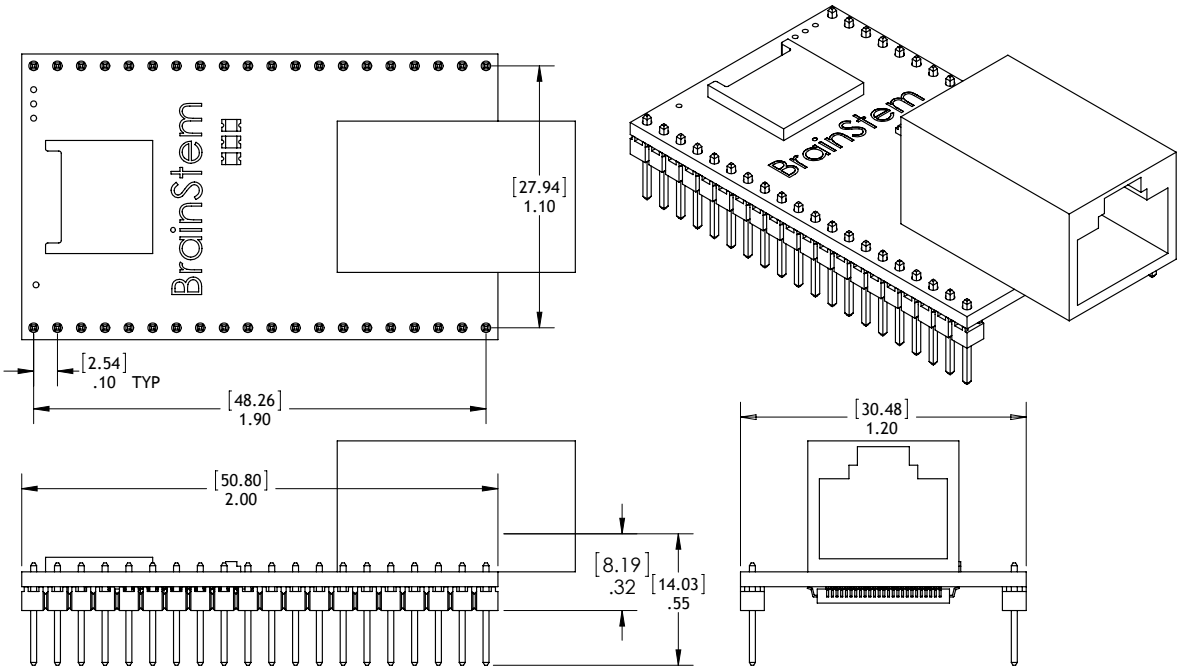


Figure 3: BrainStem EtherStem Module mechanical dimensions shown in inches [mm].

## Document Revision History

All major documentation changes will be marked with a dated revision code.

| Revision | Date | Engineer | Description |
|---|---|---|---|
| 1.0 | July 7, 2014 | MJK | Initial revision |
| 1.1 | August 27, 2014 | ECM | Updated pin mapping, absolute and recommend rating tables |