Overview

The S67-MTM-ETHERSTEM is a BrainStem® link module and is part of Acroname's Manufacturing Test Module (MTM) system. It provides an Ethernet based BrainStem link to a host PC, network or the Internet. The MTM-EtherStem forms the backbone of any system requiring general-purpose microcontroller features accessed via Ethernet and TCP/IP. A system using the MTM-EtherStem as the link module can be accessed and controlled from any network-connected device by using any one of the standard BrainStem APIs.

Features

- 3 analog to digital (A2D) inputs
- 12-bit A2D resolution; up to 200kS/s
- Up to 3kS memory depth
- 1 digital to analog converter (DAC) output
- 10-bit DAC resolution
- 15 general purpose digital inputs/outputs (DIO)
- 1 I^2C Fast Mode Plus (1 Mbps)
- 1 I^2C Fast Mode (400 kbps)
- User, link, power and heartbeat status LEDs
- 2 UART serial ports
- 1 10/100 Ethernet on standard RJ-45
- μSD slot for additional storage
- Bridge from Ethernet to I^2C bus transactions
- 6V to 12V DC wide input voltage range
- 3.3V input/output voltage
- All input/outputs protected up to 12V input
- All input/outputs reverse-polarity protected
- 0 to 70°C ambient operating temperature
- No host PC drivers required
- API support for Mac OS X, Linux and Windows

Description

The MTM-EtherStem provides general-purpose microcontroller features such as digital and analog inputs and outputs (DIOs, A2Ds, DACs) in a robust package with standard, easy to source and easy to use hardware interface connectors. It is designed and intended to be integrated directly into manufacturing test fixtures, or other measurement and data collection systems which need high-reliability, high "up-time" microcontroller interfaces. Utilizing a highly stable, wide input, linear power supply, the module can be used in noise-sensitive environments. And since the MTM-EtherStem is built on Acroname's BrainStem technology, it seamlessly integrates into larger networks of sensors and other BrainStem modules and uses powerful high-level and embedded software APIs.

Every BrainStem and MTM module utilizes the BrainStem API for C, C++ or Python based high-level applications. Modules also include the BrainStem Reflex virtual-machine, an embedded runtime engine. By using reflexes, a system can run custom, pseudo-realtime, reactive or proactive tasks without the need for a host PC or network connection. The Reflex API closely mirrors the C++ and Python APIs, making embedded application development quick and robust. Each module uses a self-discovery and notification system, allowing embedded and host based applications to determine the module's capabilities and programmatically control and direct communication between modules on the BrainStem network.

As part of Acroname's Manufacturing Test Module (MTM) system, the MTM-EtherStem is ruggedized and designed to survive the rigors of CM or OEM manufacturing environments around the world. Pin interfaces are protected against reverse polarity and over voltage conditions, and the modules operate from 0°C to 70°C ambient with no external cooling or fans.

The MTM-EtherStem's interfaces are robust against over-voltage, up to the input rail voltage, and are appropriately current limited for driving high impedance loads ($> 1k\Omega$). The DAC output can source and sink 20-30mA (see Operating Ratings).

Absolute Maximum Ratings

Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute-maximum-rated conditions for extended periods affects device reliability or may permanently damage the device.

Parameter	Minimum	Typical	Maximum	Units
Input Voltage, V_{supply}	6.0	-	14.0	V
V_{supply} current	0.0	-	120	mA
Voltage to any IO pin[1]	0.0	-	V_{supply}	

The MTM system is designed to be used in a system where V_{supply} is the highest voltage connected to all MTM modules. Each module is designed to withstand V_{supply} continuously connected to all IOs, excepting those specified above, including accidental reverse polarity connection between V_{supply} and ground (0V). As with all products, care should be taken to properly match interface voltages and use a well architected current-return path to ground for the targeted application.

Handling Ratings

Parameter	Conditions/Notes	Minimum	Typical	Maximum	Units
Ambient Operating Temperature, T_A	Non-condensing	0.0	25.0	70.0	°C
Storage Temperature, T_{STG}		-10	-	+85	°C
Electrostatic discharge, V_{ESD}	IEC 61000-4-2, level 2, contact discharge	0	-	±4000	V

Recommended Operating Ratings

The values presented apply over the full operating temperature, otherwise specifications are at T_A = 25 °C.

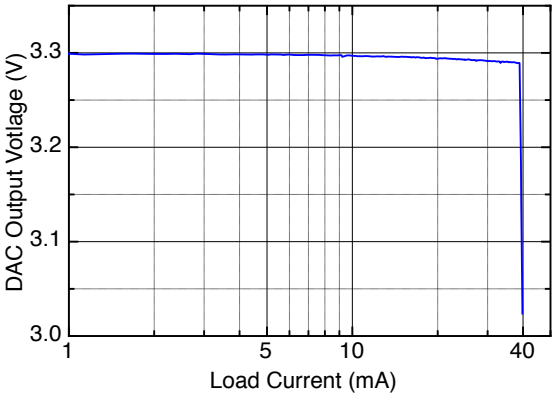
Parameter	Conditions/Notes	Min	Typical	Max	Units
Input Voltage, V_{supply}		6.0	-	12.0	V
Current Draw, I_{supply}		50	80	100	mA
Reset Low Threshold		-	1.15	-	V
I^2C SDA, SCL pins[1]		-	3.3	-	V
UART Tx/Rx Logic High, V_{IH}		1.65	-	-	V
UART Tx/Rx Logic Low, V_{IL}		-	-	1.15	V
Digital Input/Output Rail, V_{IO}		3.267	3.300	3.333	V
Digital Input Logic High, V_{IH}		1.65	-	-	V
Digital Logic Low, V_{IL}		-	-	1.15	V
Digital output source current[2]	Output set high; Shorted to GND	-	5	10	mA
Digital output sink current[2]	Output set low; connected to 3.3V	-	-5	-10	mA
Analog input impedance	100Hz	980	990	1000	kΩ
Analog input impedance	1kHz	670	680	700	kΩ
Analog input leakage current		-	3.5	-	μA
DAC output source current[3]	Output shorted to GND	25	30	35	mA
DAC output sink current[3]	Output connected to 3.3V	-15	-20	-25	mA

[1] Internal I^2C 330Ω pull-up resistors to 3.3V are always enabled.
[2] It is not recommended to continuously apply more than V_{supply} to any pin.
[3] It is not recommended to continuously apply more than 3.3V to the DAC pin for more than 5 seconds.

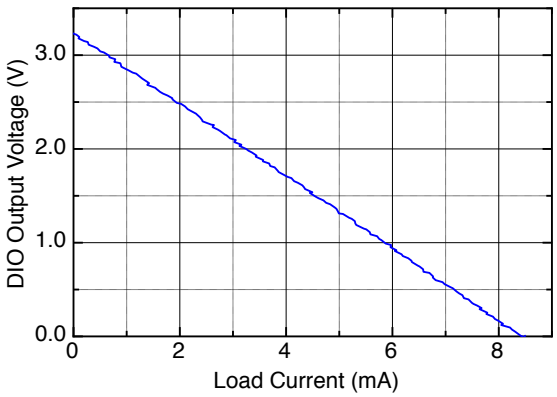
Typical Performance Characteristics

Representative of typical performance and conditions at 25°C ambient, 6.0V input supply, unless otherwise noted.

DAC 3.3V Output vs Load Current



DIO Output Voltage vs Current Load



Pin Interface

The MTM-EtherStem, like all MTM modules, use the PCIe interface connector. The MTM modules are not PCIe compliant, and will not work if installed in a PCIe-compliant card slot (this may result in damage to both connected systems). Instead, MTM modules rely on this connector for its robustness, high bandwidth, good availability and low cost. By using this interface connector, MTM modules can easily integrate into system which utilize ”throw-away” interconnect boards.

For example, in a manufacturing test system, mechanical test probes can be mounted directly on a PCB along with proper routing of electrical signals to a PCIe socket where an MTM-EtherStem is connected to execute measurements and data collection. As the device under test (DUT) changes and its test point locations change, the test-probe PCB can be discarded while keeping the MTM-EtherStem. After fabricating a new test-probe PCB, the old MTM-EtherStem is simply re-slotted into the PCIe socket, and the test system is ready to use. This model greatly reduces the time to revise test systems, and also allows for very rapid scaling of manufacturing test lines as a product goes from prototype to mass production.

MTM-EtherStem utilizes a 64 position PCIe socket like FCI’s 10018784-10201TLF.

Figure 1: 64 position PCIe socket for use with MTM-EtherStem.

Some edge connector pin designators may be omitted if no functionality is present.

Side A	Description	Notes	Side B	Description	Notes
A1	Ground		B1	Input Voltage	
A2	Ground		B2	Input Voltage	
A3	Ground		B3	Input Voltage	
A4	Ground		B4	Input Voltage	
A5	Reset	Pull to Ground to assert	B5	Input Voltage	
A6	Ground		B6	Reserved	Do not connect
A7	Ground		B7	Reserved	Do not connect
A8	I2C0 SDA (BrainStem bus)	Module includes a 330 kohm pull up resistor	B8	Ground	
A9	I2C0 SCL (BrainStem bus)	Module includes a 330 kohm pull up resistor	B9	Ground	
A10	Ground		B10	UART0 Tx	
A11	Ground		B11	UART0 Rx	
A12	Module Offset 0	Pull to Ground to set	B12	Module Offset 2	Pull to Ground to set
A13	Module Offset 1	Pull to Ground to set	B13	Module Offset 3	Pull to Ground to set

Table 1: Pin Mappings common to all MTM link modules

Side A	Description	Notes	Side B	Description	Notes
A14	Reserved	Do not connect	B14		
A15			B15		
A16			B16	UART1 Tx	
A17	I2C1 SCL	Module includes a 1kohm pull up resistor	B17	UART1 Rx	
A18	I2C1 SDA	Module includes a 1kohm pull up resistor	B18	DIO 0	
A19			B19	DIO 1	
A20			B20	DIO 2	
A21			B21	DIO 3	
A22			B22	DIO 4	
A23			B23	DIO 5	
A24	ADC0	Analog measurement only	B24	DIO 6	
A25	ADC1	Analog measurement only	B25	DIO 7	
A26			B26	DIO 8	
A27			B27	DIO 9	
A28			B28	DIO 10	
A29			B29	DIO 11	
A30			B30	DIO 12	
A31	ADC2	Analog measurement only	B31	DIO 13	
A32	ADC3	DAC output only	B32	DIO 14	

Table 2: Pin Mapping definitions unique to MTM-EtherStem

Module Software and Firmware

Module Networking

To allow for simple setup and discovery on a network, MTM-EtherStem supports DHCP for obtaining IP addresses on network. The MTM-EtherStem will automatically request a new IP address when Ethernet is connected. The MTM-EtherStem defaults to listening on IP port 8000.

The BrainStem library can search for and discover devices attached to the network. This discovery process relies on a UDP broadcast packet which may be blocked by some host operating system's firewalls or some network routers. Be sure to configure your firewall to allow broadcast packets. The discovery and connection to the MTM-EtherStem is accomplished simply through the `linkDiscoverAndConnect(linkType type)` with `linkType` of `linkType enum TCPIP`. This same interface can be used to connect to a MTM-EtherStem with a known serial number by specifying it via `linkDiscoverAndConnect(linkType type, uint32_t serialNumber)`. This discovery process is done by StemTool, which is available in the BrainStem software download.

To connect to an MTM-EtherStem at a known IP address, a the link specifier can be directly created. For example:

```
linkSpec myLinkSpec;
myLinkSpec.type = TCPIP;
myLinkSpec.serial_num = 0xABCD0123;
myLinkSpec.module = 6;
myLinkSpec.t.ip.ip_address = 0xC0A82024; //192.168.32.36
myLinkSpec.t.ip.ip_port = 8000;
```

The simplest method to obtain the information for the link specifier is to use `linkDiscoverAndConnect(TCPIP)` and then record the resulting `linkSpec` via `getLinkSpecifier()`. This link specifier can then be later used to connect to the device from other networks, assuming there is a valid TCP/IP route between the MTM-EtherStem's network and the host PC's network. StemTool also displays the relevant information needed to complete a `linkSpec` definition.

System Entities and Default Values

The MTM-EtherStem utilizes a subset of BrainStem entity implementations that are specific to the hardware's capabilities. The table below details the BrainStem API entities and macros used to interface to the MTM-EtherStem.

Parameter	Value	Implementation Macro Name	Notes
Module Definitions:			
Module Base Address	6		See Page 7
Entity Definitions:			
Analog Entity Quantity	4	aMTMBRAINSTEM_NUM_A2D	See Page 7
Digital Entity Quantity	15	aMTMBRAINSTEM_NUM_DIG	See Page 7
Store Entity Quantity	3	aMTMBRAINSTEM_NUM_STORES	See Page 7
System Entity Quantity	1		See Page 7
Timer Entity Quantity	3	aMTMBRAINSTEM_NUM_TIMERS	See Page 8

Capabilities and Interfaces

The MTM-EtherStem software is built on BrainStem® technology. The module adheres to the BrainStem protocol on I^2C and uses the BrainStem software APIs. Each functional capacity that is available on the MTM-EtherStem is described in the following sections.

Module Address

All BrainStem modules come with a specific default network I^2C base address for identification on the I^2C bus. The default module base address is factory defaulted as the value 6. This value can be changed with `system.setModule(const uint8_t address)` and saved via `system.save()` to onboard flash NVRAM. Further, link modules like the MTM-EtherStem can route traffic from the BrainStem network through the link to the host for modules that have their router address set to the address of the link module. Link modules must have their router addresses set to the same as their module address. The router address can be changed via `system.setRouter(const uint8_t address)`.

All MTM modules, like MTM-EtherStem have module address offset input pins. These pins allow for the default address to be offset by a number defined by pull-downs in the hardware. This feature makes it simple and easy to incorporate several of the same MTM module into one network without having to pre-program module addresses for each module differently. Further, in a system utilizing many of one module type, the modules may be inserted into any slot in the system without changing their software configuration. The modules will automatically apply the define module address offset when they power on, and the BrainStem network and software will then automatically discover all the modules in the network.

Analog Entities

Analog inputs and outputs entities on MTM-EtherStem are referenced to a fixed, precision 3.3V rail. Each analog input and output (AIO) pin has a current and voltage limiting circuitry to protect the pins from over voltage events. Page 3 shows a plot expected analog output (DAC) voltage as a function of current load. It is not recommended to apply more than 3.3V to any AIO pin for extended periods of time.

The supported analog entity operating modes is shown in the analog operational modes table below. AIO capabilities may change with future firmware revisions. Please contact Acroname to inquire about or request specific pin capabilities.

Analog	Input	Output	Rail
AIO0	Yes	No	3.3V
AIO1	Yes	No	3.3V
AIO2	Yes	No	3.3V
AIO3	No	Yes	3.3V

Table 3: Analog operational modes

Digital Entities

Digital inputs and outputs on MTM-EtherStem are referenced to a fixed 3.3V rail. Each digital input/output (DIO) pin has a current limiting circuit allowing driving a high-impedance ($> 1k\Omega$) loads. Page 3 shows a plot expected output voltage as a function of current load. It is not recommended to apply more than 3.3V to any DIO pin for extended periods of time.

The supported digital operating modes is shown in the digital operational modes table below. DIO capabilities may change with future firmware revisions. Please contact Acroname to inquire about or request specific pin capabilities.

Digital	Input	Output	Rail	PWM	Match
DIO0	Yes	Yes	3.3V	No	No
DIO1	Yes	Yes	3.3V	No	No
DIO2	Yes	Yes	3.3V	No	No
DIO3	Yes	Yes	3.3V	No	No
DIO4	Yes	Yes	3.3V	No	No
DIO5	Yes	Yes	3.3V	No	No
DIO6	Yes	Yes	3.3V	No	No
DIO7	Yes	Yes	3.3V	No	No
DIO8	Yes	Yes	3.3V	No	No
DIO9	Yes	Yes	3.3V	No	No
DIO10	Yes	Yes	3.3V	No	No
DIO11	Yes	Yes	3.3V	No	No
DIO12	Yes	Yes	3.3V	No	No
DIO13	Yes	Yes	3.3V	No	No
DIO14	Yes	Yes	3.3V	No	No

Table 4: Digital operational modes

Store Entities

The MTM-EtherStem supports the standard BrainStem store entity with the stores indexed as detailed in the following table.

Index	Location	Slots	Macro
0	Internal Flash	12	aMTMBRAINSTEM_NUM_INTERNAL_SLOTS
1	RAM	1	aMTMBRAINSTEM_NUM_RAM_SLOTS
2	μSD	255	aMTMBRAINSTEM_NUM_SD_SLOTS

System Entity

Every BrainStem module, including MTM-EtherStem, implements a single system entity. The system entity allows the

retrieval and manipulation of configuration settings like the module address and input voltage, control over the user LED, as well as other functionality.

Timer Entities

Timer entities provide simple scheduling for events in the reflex system. The MTM-EtherStem has 8 timers available for general purpose use. The most common usage is to have a timer reflex execute code on expiration. The simplest example is using a timer to intermittently flash an LED. A more complicated use of timers might be to have use a short time interval timer collect and log analog readings for a period of several hours, then have a long interval time relay the recorded data to a host PC or Internet server.

Block Diagram

The MTM-EtherStem Module is composed of a many different subsystems carefully linked together.

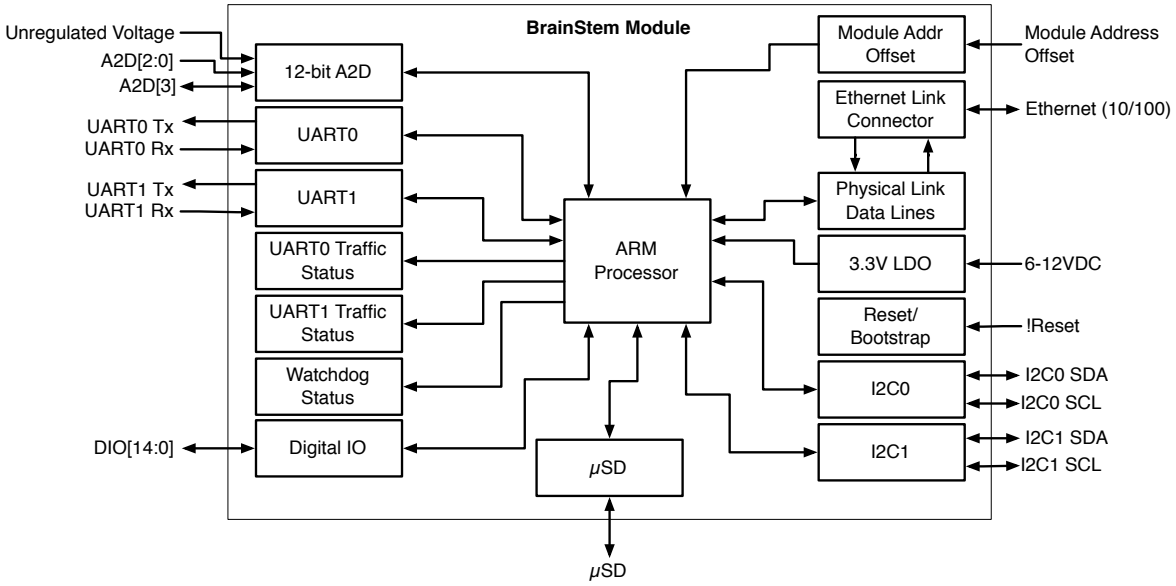
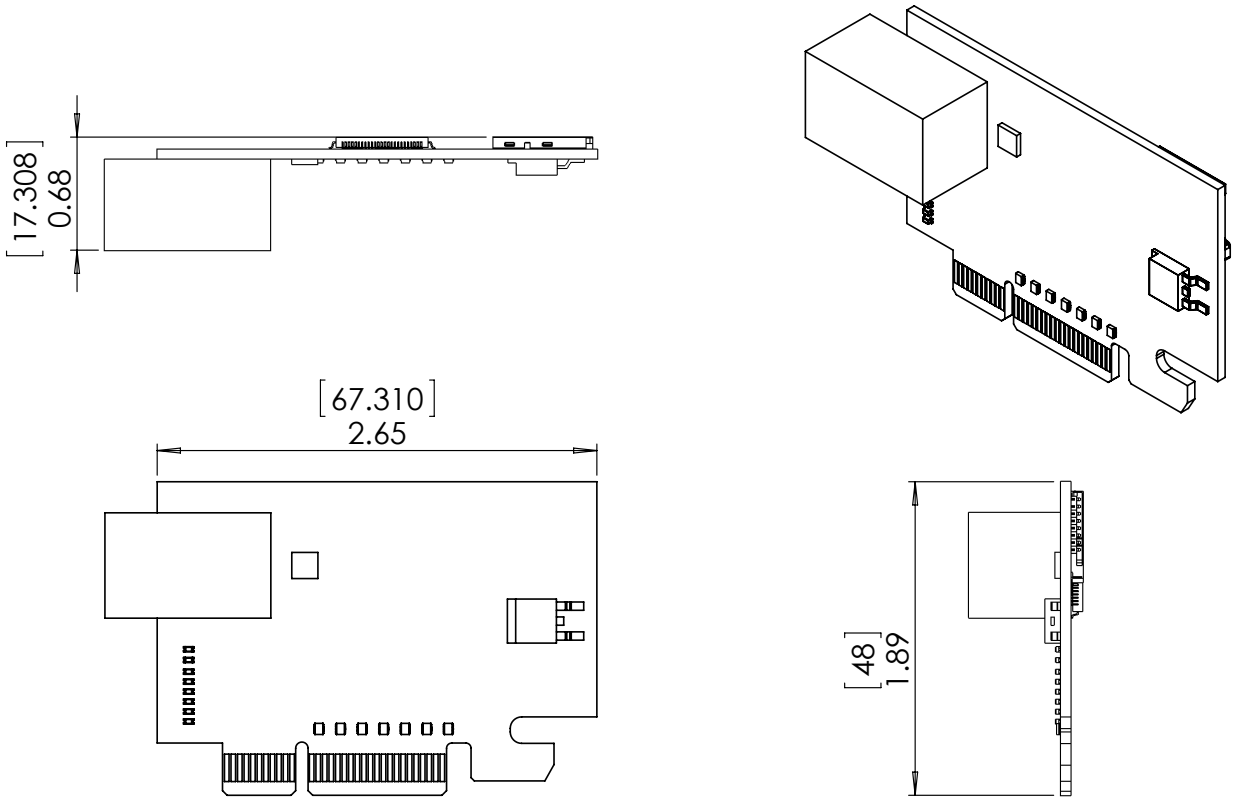


Figure 2: System block diagram

Mechanical



Document Revision History

All major documentation changes will be marked with a dated revision code.

Revision	Date	Engineer	Description
1.0	July, 2014	MJK	Initial revision
1.1	August, 2014	ECM	Updated pin map, absolute and recommended ratings
1.2	March, 2015	JLG	Updated description, features, specifications, performance data