Overview

The Acroname MTM-Relay (S78-MTM-RELAY), part of Acroname's Manufacturing Test Module (MTM) product series, is a ruggedized software-controlled SSR (Solid State Relay) module with user-accessible serial communication. The MTM-Relay allows MTM system designers to easily and modularly add relay-based power switching to their test system designs.

Ideal for use in high-reliability manufacturing or development testing environments, all features of the MTM-Relay, including relays, digital IO, and I²C communication channels are electrically protected for ESD strikes, overvoltage, over-current and short circuit conditions.

Built using Acroname's industry-proven and well-adopted BrainStem® technology, resources on the MTM-Relay are controlled via Acroname's powerful and extensible BrainStem® technology and software APIs.

Typical applications include:

– Manufacturing functional testing
– Validation testing
– Automated test development
– Embedded system development
– Power switching

Features

– 4 60V, 6A optically isolated solid state relays (NO)
– 4 overvoltage and current protected digital GPIO
– 1 BrainStem I²C FM+ (1Mbit/s) bus

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Description

The MTM-Relay module is a key component for manufacturing test and R&D of devices requiring high power switching using durable relays. For more information on the MTM platform architecture, please refer to www.acroname.com.

The MTM-Relay implements an on-board BrainStem controller running a RTOS (Real-Time Operating System), which provides a USB host connection, Independent operating capability and the BrainStem interface, for control of the MTM resources identified in this datasheet (Relay X, GPIO, etc.).

The MTM-Relay primarily provides four main software-controlled SSR relays to implement high-power switching in a test system. The relays are controlled by the BrainStem API.

Within the MTM platform architecture, the MTM-Relay module can operate either independently or as a component in a larger network of MTM modules. Each MTM-Relay is uniquely addressable and controllable from a host by connecting via the on-board USB connection, the card-edge USB input or through other MTM modules on the local BrainStem bus.

Acroname's BrainStem link is established over the selected input connection. The BrainStem link allows a connection to the on-board controller and access to the available resources in the MTM-Relay. The MTM-Relay can then be controlled via a host running BrainStem APIs or it can operate independently by running locally embedded, user-defined programs based on Acroname's BrainStem Reflex language in the RTOS.

IMPORTANT NOTE:

The MTM-Relay, like all MTM modules, utilizes a PCIe connector interface but is for use strictly in MTM-based systems – it should never be installed in a PCI slot of a host computer directly. Insertion into a PC or non-MTM system could cause damage to the PC.

Absolute Maximum Ratings

Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute-maximum rated conditions for extended periods affects device reliability and may permanently damage the device.

Parameter	Minimum	Maximum	Units
Input Voltage, V_{supply}	6.0	14.0	V
Input Current, I_{supply}	0.0	2.0	A
Voltage to any IO pin	-0.5	V_{supply}+0.5	V
Voltage to any I2C pin	0.0	5.5	V
Relay Blocking Voltage	-	60	V
Relay Input Power Dissipation (each relay)	-	150	mW
Relay Total Power Dissipation (each relay)	-	2400	mW
Relay Isolation Voltage	-	5000	V_{rms}

Table 1: Absolute Maximum Ratings

The MTM system is designed to be used in a system where V_{supply} is the highest voltage connected to all MTM modules. Each module is designed to withstand V_{supply} continuously connected to all IOs, excepting those specified above, including accidental reverse polarity connection between V_{supply} and ground (0V). As with all products, care should be taken to properly match interface voltages and ensure a well-architected current-return path to ground. As with all devices utilizing USB interfaces, care should be taken to avoid ground loops within the USB subsystem. When using the USB interface, ground must be at 0V potential to avoid damaging connected host systems.

Handling Ratings

Parameter	Conditions/Notes	Minimum	Typical	Maximum	Units
Ambient Operating Temperature, T_A	Non-Condensing	0.0	25.0	70.0	°C
Storage Temperature, T_{STG}		-10.0	-	85.0	°C
Electrostatic Discharge, V_{ESD}	IEC 61000-4-2, level 4, contact discharge	0.0	-	±8000	V

Table 2: Handling Ratings

Recommended Operating Ratings

Values presented apply to the full operating temperature range.

Parameter	Conditions/Notes	Minimum	Typical	Maximum	Units
Input Voltage, V_{supply}		6.0	-	12.0	V

Table 3: Recommended Operating Ratings

Block Diagram

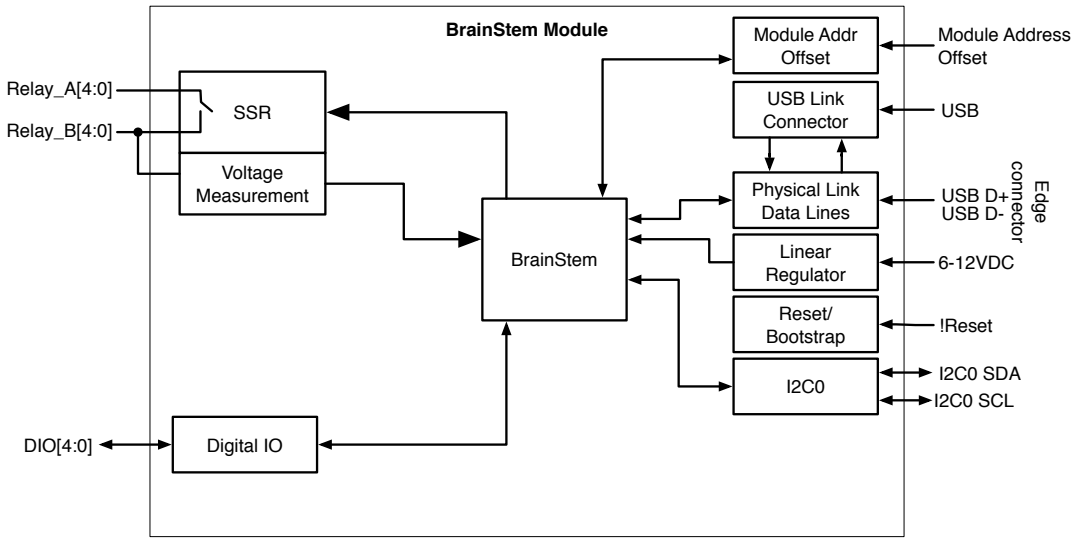


Figure 1: MTM-Relay Block Diagram

Typical Performance Characteristics

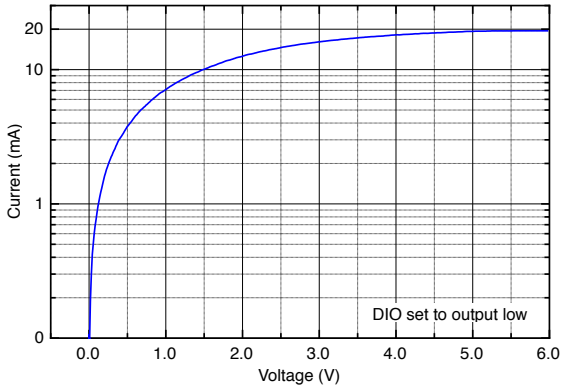
Values presented apply to the full operating temperature range.

Parameter	Conditions/Notes	Minimum	Typical	Maximum	Units
Base Current Consumption, I_{supply}	V_{supply}=6V V_{supply}=12V	- -	78 90	- -	mA
Reset Low Threshold		-	1.2	-	V
I2C SDA, SCL Pins		0.0	3.3	-	V
Digital Input Output		-	3.3	-	V
Digital Input Logic High, V_{IH}		2.15	-	-	V
Digital Input Logic Low, V_{IL}		-	-	1.1	V
Digital Output Drive Current	Output high; short to GND Output high into 2.97V	- -	20.0 3.15	30.0 -	mA
Digital Output Sink Current	Output low; short to V_{supply}	-	-20.0	-30.0	mA
Digital Output Short Duration	Output high	-	Infinite	-	hours
Digital Output Overvoltage	V_{supply} on pin	-	Infinite	-	hours
Digital Input Resistance	Configuration mode set to both Input and High-Z	-	4.25	4.45	MΩ
Digital Input Leakage Current	Configuration mode set to both Input and High-Z	-	110	-	µA
Digital Sample Rate[1]	Mac OS X Windows 10 Linux – 14.04 LTS Reflex	- - - -	700 1000 850 8200	1000 1000 1000 -	Hz
Digital Output Jitter	Using Reflex only Reflex w/ BrainStem load	- -	- -	25 100	µS µS
Relay Load Current, Continuous, I_L	Free air	-	-	6	$\pm A_{DC}$, A_{rms}
Relay Peak Load Current, I_{LPK}	t = 10ms	-	-	20	$\pm A_P$
Relay On-Resistance, R_{ON}	I_L = 1A	-	-	0.06	Ω
Relay Off-State Leakage Current, I_{LEAK}	V_L = 60V	-	-	1	µA
Relay Switching Speeds Turn-On, t_{ON} Turn-Off, t_{OFF}	I_L=100mA	 900 10	 1300 14	 1700 18	µs
Relay Output Capacitance, C_{OUT}	V_L=50V, f=1MHz	-	340	-	pF
Relay Voltage Measurement Error		-	±1.0	±2.0	%

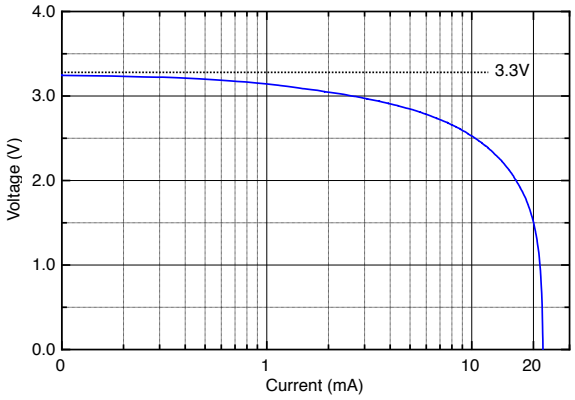
[1] Host dependent, test was done as a single instruction, subsequent instructions may affect performance. Measurements taken using BrainStem Library 2.3.2. The Nyquist frequency should be considered when referring to these values.

Table 4: Typical Performance Characteristics

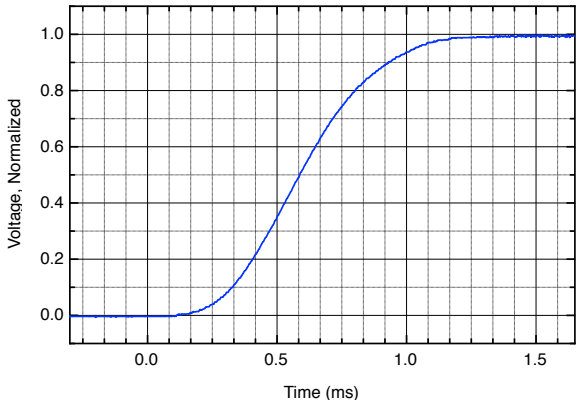
DIO Output Sink Current vs. Applied Voltage



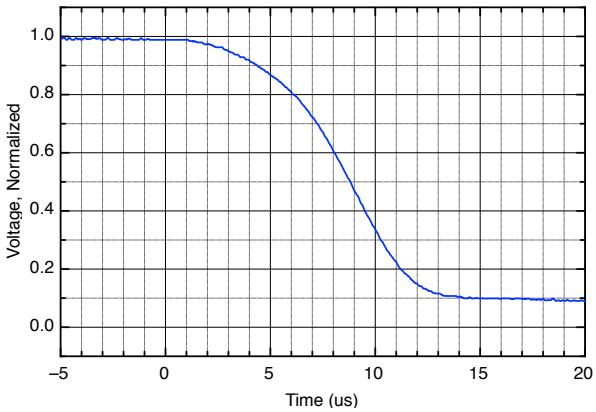
DIO Output High Voltage vs. Current Load



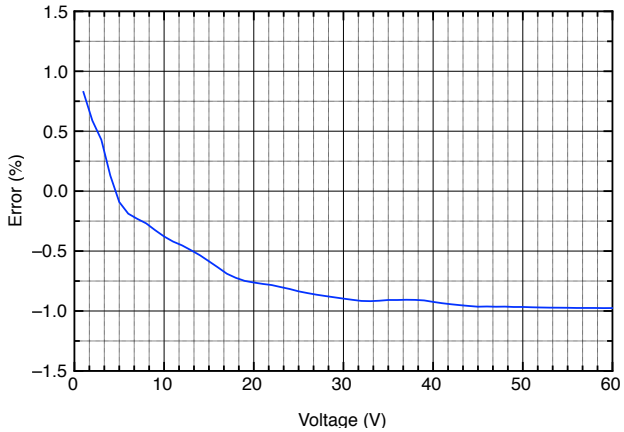
Relay Voltage Rise Time, Normalized



Relay Voltage Fall Time, Normalized



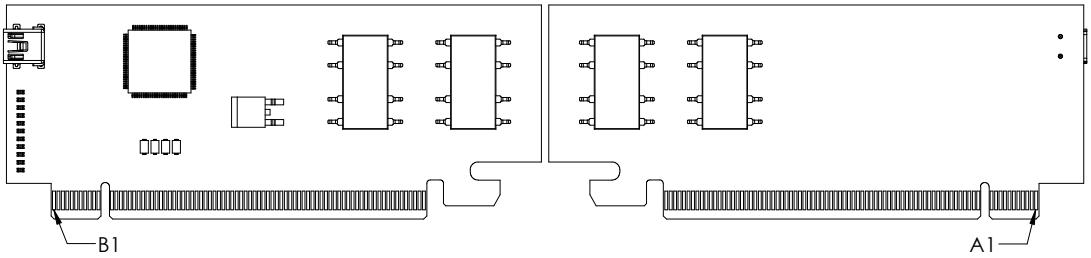
Typical Relay Voltage Measurement Error



Pinout Descriptions

WARNING: Acroname's MTM line features a PCIe connector that is common in most desktop computers; however, they are NOT intended nor designed to work in these devices. Do NOT insert this product into any PCIe slot that wasn't specifically designed for this product! Failure to follow this warning WILL result in damage to this product and any device you connect it to.

The MTM edge connector pin assignments are shown in the following table. Please refer to Table 3: Recommended Operating Ratings for appropriate signal levels.



Pins Common to all MTM Modules

Edge Connector Side A	Edge Connector Side A Description	Edge Connector Side B	Edge Connector Side B Description
1	GND	1	Input Voltage, V_{supply}
2	GND	2	Input Voltage, V_{supply}
3	GND	3	Input Voltage, V_{supply}
4	GND	4	Input Voltage, V_{supply}
5	Reset	5	Input Voltage, V_{supply}
6	GND	6	Reserved, Do Not Connect
7	GND	7	Reserved, Do Not Connect
8	I^2C0 SCL	8	GND
9	I^2C0 SDA	9	GND
10	GND	10	Reserved, Do Not Connect
11	GND	11	Reserved, Do Not Connect
12	Module Address Offset 0	12	Module Address Offset 2
13	Module Address Offset 1	13	Module Address Offset 3

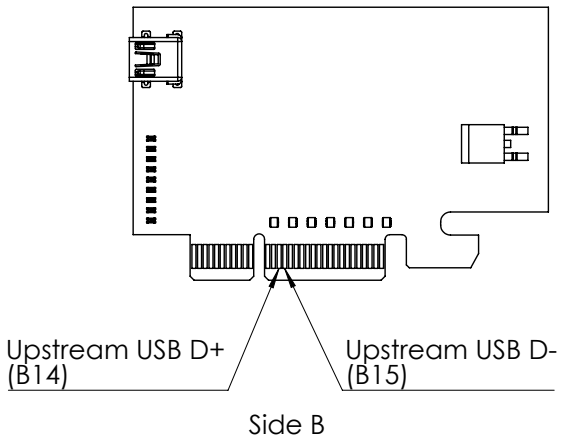
Pins Specific to MTM-Relay

Edge Connector Side A	Edge Connector Side A Description	Edge Connector Side B	Edge Connector Side B Description
14	Reserved, Do Not Connect	14	USB Upstream Data +
15	Reserved, Do Not Connect	15	USB Upstream Data -
16	Reserved, Do Not Connect	16	Reserved, Do Not Connect
17	Reserved, Do Not Connect	17	Reserved, Do Not Connect
18	Digital IO 1	18	Digital IO 0
19	Digital IO 3	19	Digital IO 2
20:49	Reserved, Do Not Connect	20:49	Reserved, Do Not Connect
50	GND	50	Reserved (24V)
51	GND	51	Reserved (24V)
52	GND	52	Reserved (24V)
53	Reserved, Do Not Connect	53	Reserved, Do Not Connect
54	Reserved, Do Not Connect	54	Reserved, Do Not Connect
55	Reserved, Do Not Connect	55	Reserved, Do Not Connect
56	Reserved, Do Not Connect	56	Reserved, Do Not Connect
57	Reserved, Do Not Connect	57	Reserved, Do Not Connect
58	Reserved, Do Not Connect	58	Reserved, Do Not Connect
59	Reserved, Do Not Connect	59	Reserved, Do Not Connect
60	Relay 0, A	60	Relay 2, A
61	Relay 0, A	61	Relay 2, A
62	Relay 0, A	62	Relay 2, A
63	Reserved, Do Not Connect	63	Reserved, Do Not Connect
64	Reserved, Do Not Connect	64	Reserved, Do Not Connect
65	Relay 0, B	65	Relay 2, B
66	Relay 0, B	66	Relay 2, B
67	Relay 0, B	67	Relay 2, B
68	Reserved, Do Not Connect	68	Reserved, Do Not Connect
69	Reserved, Do Not Connect	69	Reserved, Do Not Connect
70	Reserved, Do Not Connect	70	Reserved, Do Not Connect
71	Reserved, Do Not Connect	71	Reserved, Do Not Connect
72	Reserved, Do Not Connect	72	Reserved, Do Not Connect

73	Reserved, Do Not Connect	73	Reserved, Do Not Connect
74	Reserved, Do Not Connect	74	Reserved, Do Not Connect
75	Relay 1, A	75	Relay 3, A
76	Relay 1, A	76	Relay 3, A
77	Relay 1, A	77	Relay 3, A
78	Reserved, Do Not Connect	78	Reserved, Do Not Connect
79	Reserved, Do Not Connect	79	Reserved, Do Not Connect
80	Relay 1, B	80	Relay 3, B
81	Relay 1, B	81	Relay 3, B
82	Relay 1, B	82	Relay 3, B

Upstream USB Connectivity Options

All MTM modules with upstream USB connections (that's all MTM excluding MTM-EtherStem) have two methods for connection via USB: through the Mini-B connector, or through pins B14 and B15 of the PCIe edge connector (below). The upstream mode defaults to AUTO, which prioritizes based on the presence or absence of VBUS at the Mini-B connector.



Module Hardware and Software Default Values

The MTM-Relay module utilizes a subset of BrainStem entity implementations that are specific to the hardware's capabilities. Table 5: MTM-Relay Hardware and Software Default Values details the BrainStem API entities and macros used to interface to the MTM-Relay module. For C and C++ developers, these macros are defined in `aMTMRelay.h` from the BrainStem development package. For Python development, the module `MTMRelay` class defines the extent of each entity array.

While the BrainStem API entities define the full potential functionality of a given interface, not all features are supported by the MTM-Relay module. Table 5: MTM-Relay Hardware and Software Default Values defines each of the options implemented with each entity, which varies by entity index. Calling an unsupported entity option will return an appropriate error (e.g.: `aErrInvalidEntity`, `aErrInvalidOption`, `aErrMode`, or `aErrUnimplemented`) as defined in `aError.h` for C and C++ and the `Result` class in Python.

Parameter	Index	Macro Name or Implemented Options	Notes
Module Definitions:			
Module Base Address	10	aMTM_RELAY_MODULE _ADDRESS	See aMTMRelay.h
Entity Class Definitions:			
`relay` Entity Quantity	4	aMTM_RELAY_NUM_RELAYS	
`digital` Entity Quantity	4	aMTM_RELAY_NUM_DIG	
`i2c` Entity Quantity	1		
`Store` Entity Quantity	2	aMTM_RELAY_NUM_STORES	
`system` Entity Quantity	1		
`timer` Entity Quantity	8	aMTM_RELAY_NUM_TIMERS	

Table 5: MTM-Relay Hardware and Software Default Values[2]

[2] Refer to `aMTMRelay.h` within the BrainStem Development Kit download for actual file.

Capabilities and Interfaces

The MTM-Relay module software is built on Acroname's BrainStem technology. The module adheres to the BrainStem protocol on I²C and uses BrainStem software APIs. For the most part, functionality that is unique to the MTM-Relay is described in the following sections; refer to Table 6: Supported MTM-Relay BrainStem Entity API Methods for a complete list of all available API functionality. All shortened code snippets are loosely based on the C++ method calls – Python and Reflex are virtually the same. Please consult the BrainStem Reference for implementation details[3].

System Entities

Every BrainStem module includes a single System Entity. The System Entity allows access to configuration settings such as the module address, input voltage, control over the user LED and many more.

Saving Entity Settings

Some entities can be configured and saved to non-volatile memory. This allows a user to modify the startup and operational behavior for the MTM-Relay away from the factory default settings. Saving system settings preserves the settings to become the new default. Most changes to system settings require a save and reboot before taking effect. Use the following command to save changes to system settings before reboot:

```
stem.system.save()
```

Saved Configurations	
Software Offset	I2C Rate
Router Address	Boot Slot
Heartbeat Rate	

Store Entities

Every BrainStem module includes several Store entities and on-board memory slots to load Reflex files (for details on Reflex, see BrainStem Reference online http://acroname.com/entities/index.html). One Reflex file can be stored per slot. Store[0] refers to the internal memory, with 12 available slots, and store[1] refers to RAM, with 1 available slot.

Digital Entities

The MTM-Relay has four (4) digital input/outputs (DIO) controlled by the digital entity. Each DIO is controllable via software and is independently current limited for both source and sink currents.

All DIO are input and output capable.

```
stem.digital[0].setConfiguration(mode)
stem.digital[0].getConfiguration(mode)
```

The *mode* parameter is an integer that correlates to the following:

- 0 (digitalConfigurationInput)
- 1 (digitalConfigurationOutput)
- 4 (digitalConfigurationHiZ)

If a digital pin is configured as output mode, setting the digital logic level:

```
stem.digital[0].setState(level)
```

If a digital pin is configured as input mode, reading the digital logic level:

```
stem.digital[0].getState(level)
```

If a digital pin is configured in HighZ mode its internal circuitry has been disconnected to create a high impedance. There are no functions that can act on this configuration.

Digital	Input	Output	HighZ	RCServo
DIO0	Yes	Yes	Yes	None
DIO 1	Yes	Yes	Yes	None
DIO 2	Yes	Yes	Yes	None
DIO 3	Yes	Yes	Yes	None

Relay Entities

The MTM-Relay has four (4) optically isolated solid-state relays controlled by the relay entity. Each relay is controllable via software and capable of 60V and 6A continuous current load.

The relay entity also includes a load voltage measurement feature, allowing the load voltage measurement to be taken with reference to GND any time the relay is enabled.

Enabling the relay:

```
stem.relay[0].setState(state)
```

Reading the load voltage value:

```
stem.relay[0].getVoltage(value)
```

I²C Entities

The MTM-Relay includes access to a single I²C bus operating at a set 1Mbit/s rate.

NOTE: The 1Mbit/s bus, while user-accessible, is also used for primary BrainStem communication so there may be other, non-user-initiated traffic as well, particularly with linked BrainStem units.

The maximum data size for individual `read` and `write` operations on an I²C bus through the BrainStem API is 20 bytes. Sending more than 20 bytes of information has to be done as an iterated sequence. For example, sending 2 bytes (0xBEEF) through the I²C bus to a device with an address 0x42 would be written:

```
stem.i2c.write(0x42, 2, 0xBEEF)
```

Reading 2 bytes of data from a device with an address 0x42 would be written:

```
stem.i2c.read(0x42, 2, buffer)
```

Where *buffer* would be a char array in C++.

Each I²C bus also includes 330Ω pull-up resistors on the SDA and SCL lines which should allow for reliable bus communication upto 1Mbps (FastMode+).

MTM-Relay Supported Entity Methods Summary

Detailed entity class descriptions can be found in the BrainStem Reference (http://acroname.com/entities/index.html). A summary of MTM-Relay class options are shown below. Note that when using Entity classes with a single index (aka, 0), the index parameter can be dropped. For example:

```
stem.system[0].setLED(1) → stem.system.setLED(1)
```

Entity Class	Entity Option	Variable(s) Notes
digital[0-3]	setConfiguration	
	getConfiguration	
	setState	
	getState	
i2c[0]	write	
	read	
relay[0-3]	setState	
	getState	
	getVoltage	
store[0-2]	getSlotState	
	loadSlot	
	unloadSlot	
	slotEnable	
	slotDisable	
	slotCapacity	
	slotSize	
system[0]	save	
	reset	
	setLED	
	getLED	
	setBootSlot	
	getBootSlot	

	getInputVoltage	
	getVersion	
	getModuleBaseAddress	
	getModuleSoftwareOffset	
	setModuleSoftwareOffset	
	getModuleHardwareOffset	
	setHBInterval	
	getHBInterval	
	getRouterAddressSetting	
	getModule	
	getSerialNumber	
	setRouter	
	getRouter	
	getModel	
	routeToMe	
timer[0-8]	getExpiration	
	setExpiration	
	getMode	
	setMode	

Table 6: Supported MTM-Relay BrainStem Entity API Methods[3]

[3] See BrainStem software API reference at https://acroname.com/reference/ for further details about all BrainStem API methods and information.

LED Indicators

The MTM-Relay board has a number of LED indicators to assist with MTM system development, debugging, and monitoring. These LEDs are shown in the diagrams below.

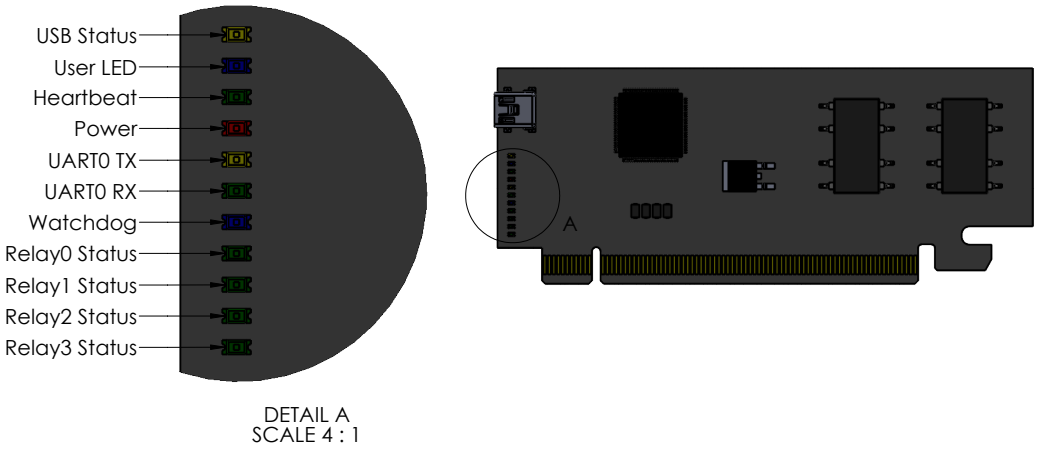


Figure 2: MTM-Relay LED Indicators

Edge Connector Interface

All MTM products are designed with an edge connector interface that requires a compatible edgeboard connector on the carrier PCB. Acroname recommends the through-hole PCI-Express (PCIe) Vertical Connector. The connectors can be combined with an optional retention clip, as shown below.

MTM Product	Manufacturer	Manufacturer Part Number	Description
MTM-Relay	Amphenol FCI Samtec	10018784-10203TLF PCIE-164-02-F-D-TH	PCI-Express 164-position vertical connector
MTM-IO-Serial	Amphenol FCI Samtec	10018784-10202TLF PCIE-098-02-F-D-TH	PCI-Express 98-position vertical connector
MTM-PM-1	Amphenol FCI Samtec	10018784-10201TLF PCIE-064-02-F-D-TH	PCI-Express 64-position vertical connector
MTM-USBStem	Amphenol FCI Samtec	10018784-10201TLF PCIE-064-02-F-D-TH	PCI-Express 64-position vertical connector
MTM-EtherStem	Amphenol FCI Samtec	10018784-10201TLF PCIE-064-02-F-D-TH	PCI-Express 64-position vertical connector
All Models	Amphenol FCI	10042618-003LF	PCI-Express Retention Clip (optional)

Table 7: PCI-Express Edge Connectors for MTM Products

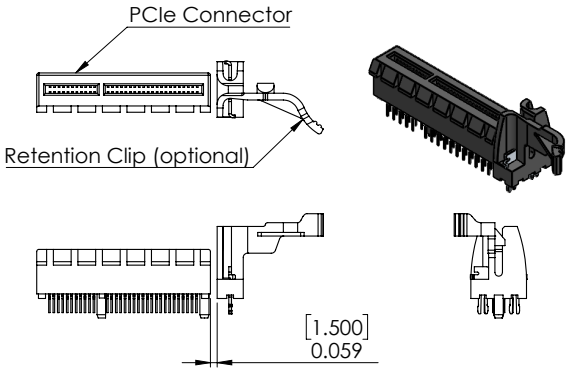


Figure 3: PCIe Vertical Connector with optional Retention Clip

MTM Edge Connector Specifications	Description
Contact Finish	Gold
Card Thickness	0.0625" [1.59mm]
Number of Rows	2
Number of Positions	Variable (see Table 7: PCI-Express Edge Connectors for MTM Products)
Pitch	0.039" (1.00mm)

Table 8: MTM Edge Connector Specifications

Amphenol FCI Drawings and Layout: http://portal.fciconnect.com/Comergent//fci/drawing/10018784.pdf

Amphenol FCI Product Specification: http://portal.fciconnect.com/res/en/pdffiles/Specs/gs-12-233.pdf

Samtec Product Catalog: http://suddendocs.samtec.com/catalog_english/pcie.pdf

Mechanical

Dimensions are shown in inches [mm]. 3D CAD models are available through the MTM-Relay product page's Downloads section.

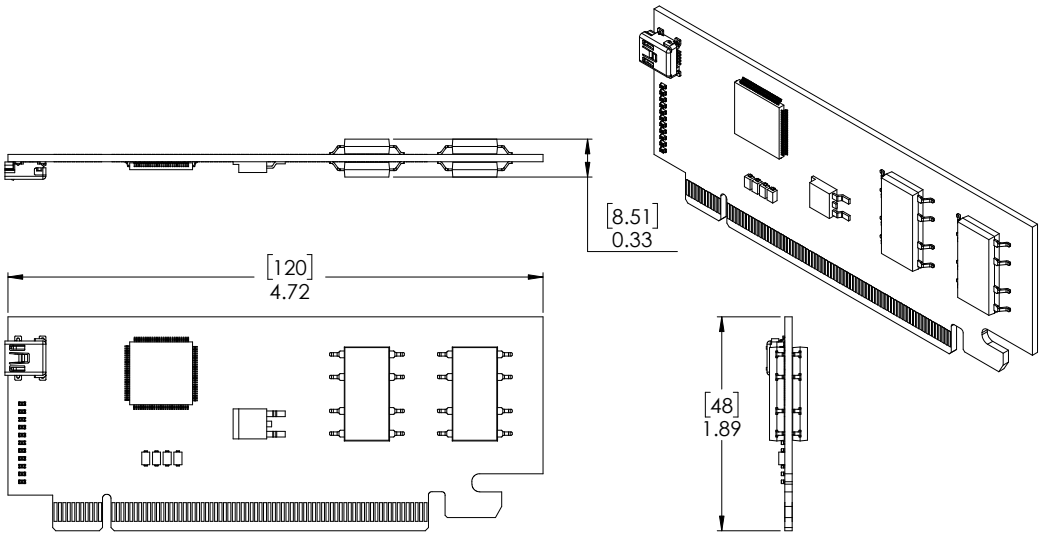


Figure 4: MTM-Relay Mechanical

Module Address Hardware Offset Configuration

A hardware offset is one of two ways to modify the module's address on the BrainStem network. Using hardware offset pins is useful when more than one of the same type of module is installed on a single BrainStem network. Applying a different hardware offset to each module of the same type in one network allows for all the modules to seamlessly and automatically configure the network for inter-module communication. Further, modules can be simply swapped in and out of the network without needing to pre-configure a module's address before being added to a network. Finally, when a system has more than one of the same type of module in a network, the module address hardware offset can be used to determine the module's physical location and thus its interconnection and intended function. For detailed information on BrainStem networking see the reference guide.

Each hardware offset pin can be left floating or pulled to ground with a 1kΩ resistor or shorted to ground. Pin states are only read when the module boots, either from a power cycle, hardware or software reset. The hardware offset pins are treated as an inverted binary number which is multiplied by 2 and added the to the module's base address. The hardware offset calculation is detailed in the following table.

HW Offset Pin				Address Offset	Module Base Address	Final Module Address
0	1	2	3			
NC	NC	NC	NC	0	4	4
1	NC	NC	NC	2	4	6
NC	1	NC	NC	4	4	8
NC	NC	1	NC	8	4	12
NC	NC	NC	1	16	4	20
1	NC	NC	1	4+16	4	24

Document Revision History

All major documentation changes will be marked with a dated revision code

Revision	Date	Engineer	Description
1.0	April 2016	JTD	Initial Revision
1.1	May 2016	JTD	Fixed pin mapping
1.2	September 2016	RMN	Formatting, Error checking, updates
1.2.1	October 2016	LCD	Update Overview, Features, Description, added DO jitter
1.3	December 2016	JG	Clarified I2C pull-ups; update supported API calls