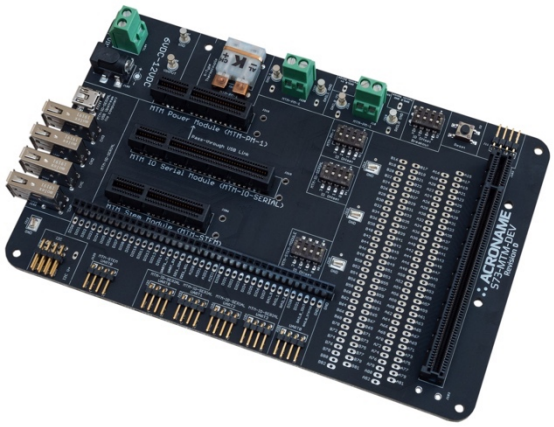

Overview

The MTM Development Board 1.0 (S73-MTM-DEV), as part of the Acroname® MTM (Manufacturing Test Module) product series, is a connectivity solution designed for development or integration to wire-based testers. The MTM-DEV-1 allows MTM system designers to easily and quickly access MTM module resources through direct soldering, 0.1” headers or application specific connections.

Ideal for use in high-reliability manufacturing or development testing environments, MTM-DEV-1 exposes all standard features of the MTM-PM-1, MTM-IO-SERIAL, MTM-USBSTEM, and MTM-ETHERSTEM modules plus it includes one policy-free slot for an additional MTM.

Built using Acroname’s industry-proven and well-adopted BrainStem® technology, resources on the MTM modules installed in the MTM-DEV-1 are controlled via Acroname's powerful and extensible BrainStem technology and software APIs.

Typical Application

– Manufacturing functional testing

– Validation testing

– Automated test development

– Embedded system development

System Features

– 1 MTM-PM-1 module slot

– 1 MTM-IO-SERIAL module slot

– 1 MTM-USBSTEM or MTM-ETHERSTEM module slot

– 1 policy-free MTM module slot

– BrainStem network connection between slots

– DIP switches to customize BrainStem addresses

– 6-12V power input via barrel jack or screw terminals

– BrainStem bus connection for expansion

– Pin access to MTM resources on all MTM slots

– Customizable to support direct wire soldering, terminal style connectors, or application specific connections

Description

The MTM-DEV-1 breakout board is a convenient component for manufacturing test solutions developing or implementing MTM using wired connections. BrainStem interface and APIs are at https://acroname.com/reference.

The MTM-DEV-1 implements one slot each for MTM-PM-1, MTM-IO-SERIAL, MTM-USBSTEM/MTM-ETHERSTEM, and one policy-free MTM slot to accommodate any additional MTM module.

The high-density connections of the MTM modules are broken out to low-density connectors, 0.1” spaced headers, and peripheral specific connections. The headers and connectors can be routed in a customized manner for the connectivity needed in a given test system.

Modules installed in MTM-DEV-1 are networked together via a local I2C-based BrainStem network. DIP switches near each slot allow custom addressing of each module on the BrainStem network. One optional connector on MTM-DEV-1 allows the BrainStem network to be expanded to other BrainStem enabled devices or development boards. Features of any MTM modules installed are easily controlled via the BrainStem API.

Within the MTM platform architecture, any MTM module can operate either independently or as a component in a larger network of MTM modules. Each module is uniquely addressable and controllable from a host by connecting via the on-board USB connection, the module’s card-edge USB input or through other MTM modules on the local MTM/BrainStem I2C bus.

IMPORTANT NOTE:

The MTM-DEV-1 utilizes a PCIe connector interface but is for use strictly in MTM-based systems. It should never be installed in a PCI slot of a host computer directly. Insertion into a PC or non-MTM system could cause damage to the PC.

Absolute Maximum Ratings

Any ABSOLUTE MAXIMUM RATINGS for MTM-DEV-1 will be specific to the MTM modules installed. Please refer to the datasheets related to specific MTM modules for the relevant ABSOLUTE MAXUMUM RATINGS.

Block Diagram

Showing populated and not populated (NP) connectors

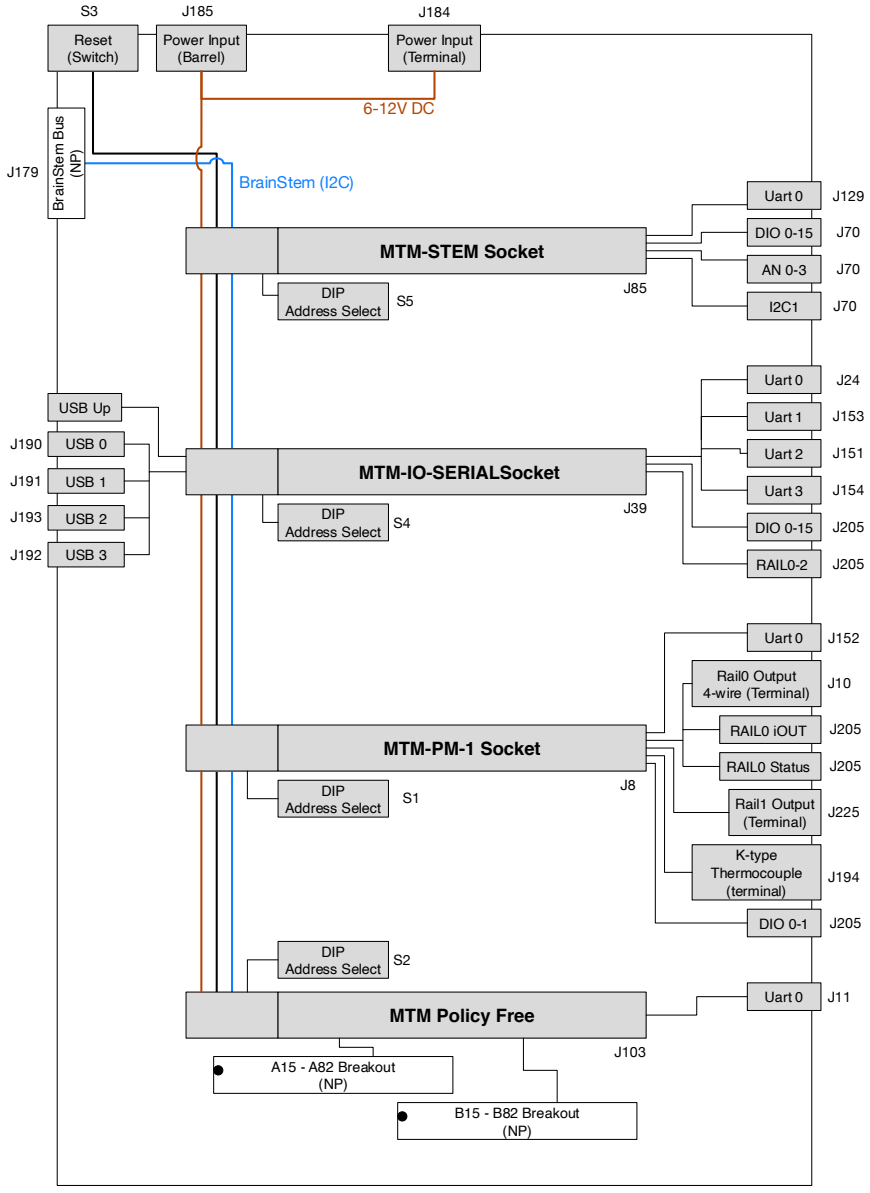

Figure 1: MTM-DEV-1 Block Diagram

Pinout Descriptions

WARNING: Acroname's MTM line features a PCIe connector that is common in most desktop computers; however, they are NOT intended nor designed to work in these devices. Do NOT insert this product into any PCIe slot that wasn't specifically designed for this product! Failure to follow this warning WILL result in damage to this product and any device you connect it to.

The MTM edge connector pin assignments are shown in the following table.

An example MTM module is shown below:

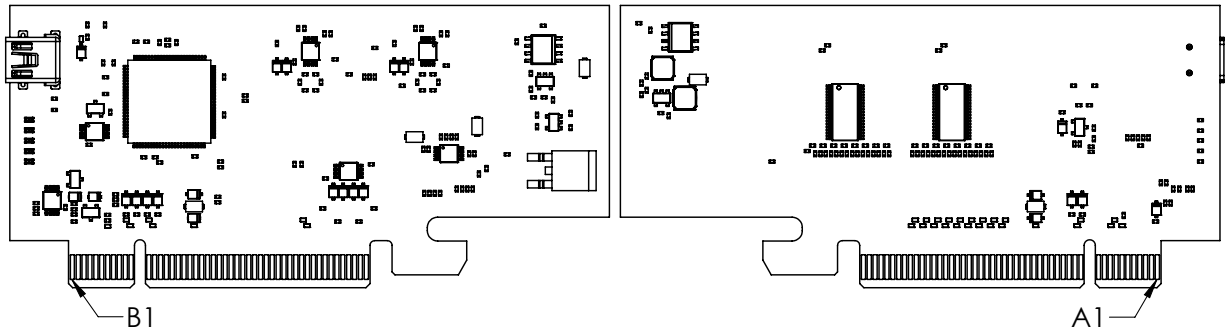

Figure 2: MTM A/B Sides

J85, J39, J8, J103: MTM Sockets (pins common to all modules)

Edge Connector Side A	Edge Connector Side A Description	Breakout A1	Edge Connector Side B	Edge Connector Side B Description	Breakout B1
A1	GND	1	B1	Input Voltage, V_{supply}	-
A2	GND	2	B2	Input Voltage, V_{supply}	-
A3	GND	-	B3	Input Voltage, V_{supply}	-
A4	GND	-	B4	Input Voltage, V_{supply}	-
A5	Reset[2]	All MTM, RST Button	B5	Input Voltage, V_{supply}	-
A6	GND	-	B6	Reserved, Do Not Connect	-
A7	GND	-	B7	Reserved, Do Not Connect	-
A8	I²C0 SCL[1]	3	B8	GND	-
A9	I²C0 SDA[1]	4	B9	GND	-
A10	GND	-	B10	Reserved, Do Not Connect	-
A11	GND	-	B11	Reserved, Do Not Connect	-
A12	Module Address Offset 0	MTM SW0	B12	Module Address Offset 2	MTM SW2
A13	Module Address Offset 1	MTM SW1	B13	Module Address Offset 3	MTM SW3

[1] I²C0 SCL and SDA nets are connected to all MTM module sockets and the BrainStem bus connectors (not populated)
[2] Reset net is connected to all MTM module sockets and the reset push button (not populated)

MTM Policy Free Socket pinout

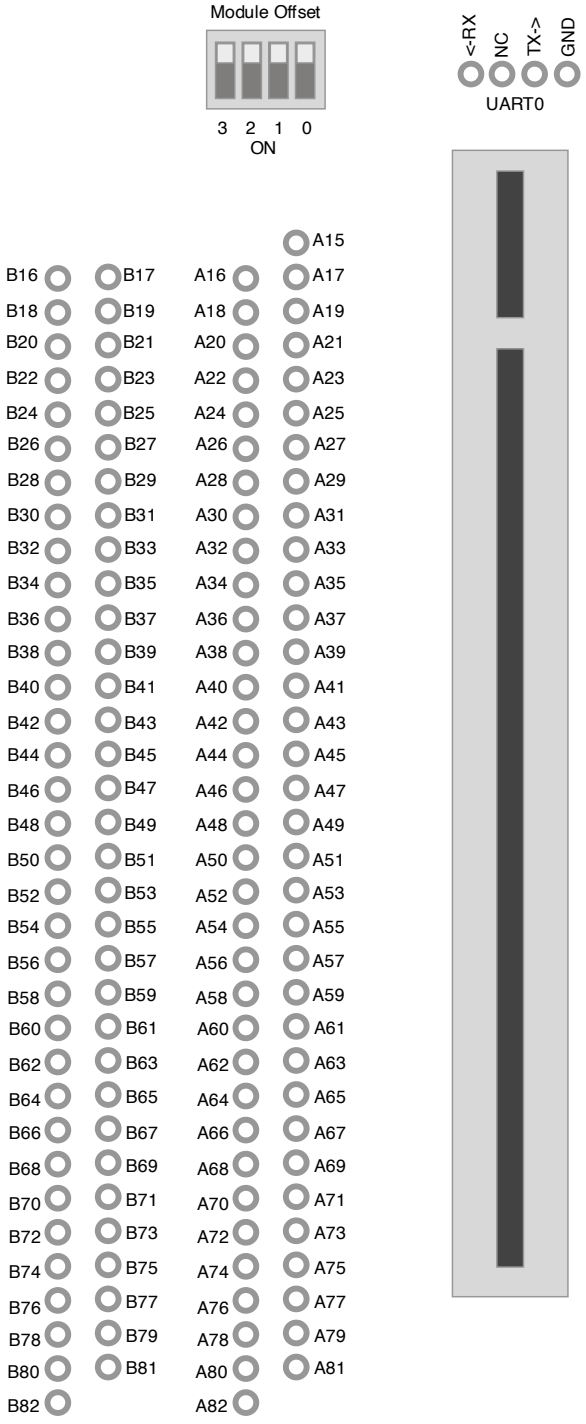

Figure 3: MTM Policy Free Socket Pinout

2-pin Terminal: MTM-PM-1 Rail 0-1 (J10, J225)

Pin	Description
1	Rail v+
2	GND

Table 7: Pinout for Terminal PM1 Rail Connectors

2-pin Barrel: Power (J185)

Pin	Description
1	Center / Vsupply
2	Ring / GND
3	Ring / GND

Table 8: Pinout for Barrel Power Connector

2-pin Terminal: Power (J184)

Pin	Description
1	Vsupply
2	GND

Table 9: Pinout for Terminal Power Connector

2 row 4pin 0.1: BrainStem I2C (J179)

Pin	Description
1	GND
2	GND
3	SCL
4	SCL
5	Reserved (I2C V+)
6	Reserved (I2C V+)
7	SDA
8	SDA

Table 10: Pinout for BrainStem I2C Connectors

4pin 0.1: UART (J11,J24,J129,J151,J152,J153,J154):

Pin	Description
1	GND
2	TX
3	NC
4	RX

Table 11: Pinout for MTM Socket UART Connectors

K-type Thermocouple (J134):

Pin	Description
1	CH +
2	AL -

Table 12: Pinout for K-Type Thermocouple.

Module Connectivity

BrainStem:

Module slots on MTM-DEV-1 are connected together using the BrainStem bus through I2C0 on pins A8 and A9 of the PCIe edge connector. The BrainStem bus is accessible through J179 connectors for external access or expansion to other BrainStem enabled devices.

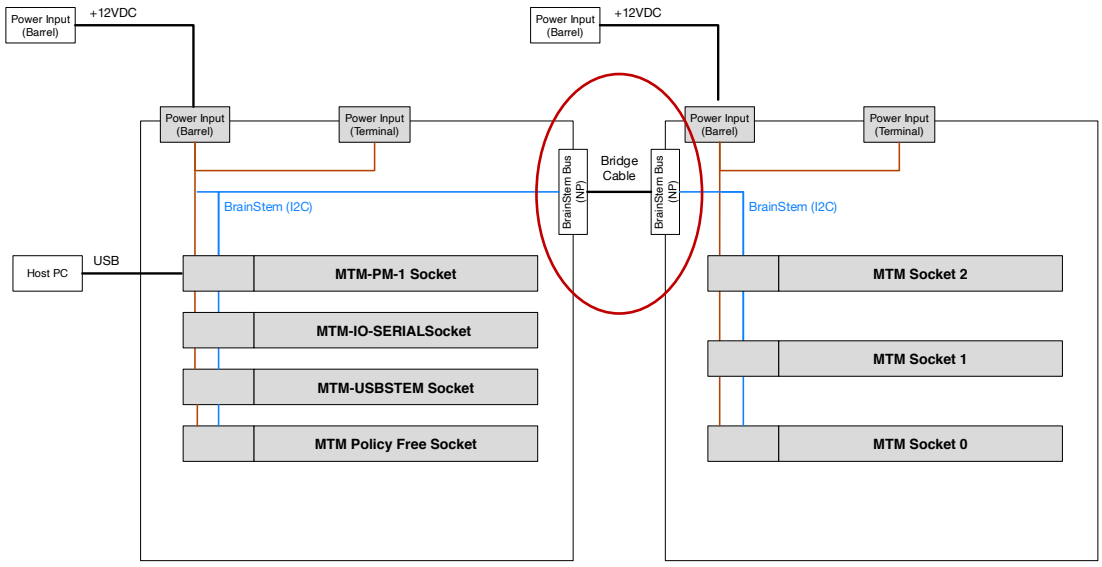

Figure 2: Bridging multiple MTM-DEV-1 boards using BrainStem

MTM Edge Connector Interface

All MTM products are designed with an edge connector interface that requires a compatible edgeboard connector on the carrier PCB. Acroname recommends the through-hole PCI-Express (PCIe) Vertical Connector. The connectors can be combined with an optional retention clip, as shown below. MTM-DEV-1 is populated with 164-position connectors which accept any MTM module.

MTM Product	Manufacturer	Manufacturer Part Number	Description
MTM Policy Free	Amphenol FCI Samtec	10018784-10203TLF PCIE-164-02-F-D-TH	PCI-Express 164-position vertical connector
MTM-IO-Serial	Amphenol FCI Samtec	10018784-10202TLF PCIE-098-02-F-D-TH	PCI-Express 98-position vertical connector
MTM-PM-1	Amphenol FCI Samtec	10018784-10201TLF PCIE-064-02-F-D-TH	PCI-Express 64-position vertical connector
MTM-USBStem	Amphenol FCI Samtec	10018784-10201TLF PCIE-064-02-F-D-TH	PCI-Express 64-position vertical connector
MTM-EtherStem	Amphenol FCI Samtec	10018784-10201TLF PCIE-064-02-F-D-TH	PCI-Express 64-position vertical connector
All Models	Amphenol FCI	10042618-003LF	PCI-Express Retention Clip (optional)

Table 1: PCI-Express Edge Connectors for MTM Products

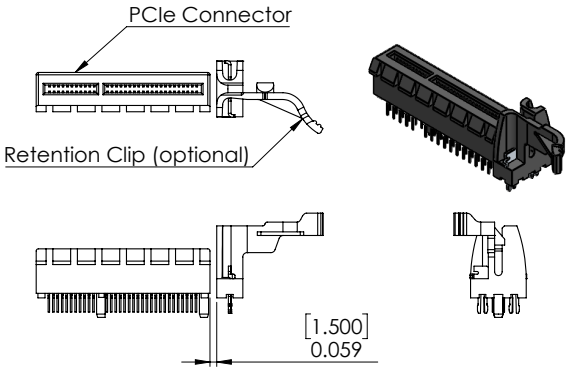

Figure 3: PCIe Vertical Connector with optional Retention Clip

MTM Edge Connector Specifications	Description
Contact Finish	Gold
Card Thickness	0.0625” [1.59mm]
Number of Rows	2
Number of Positions	Variable (see Table 1: PCI-Express Edge Connectors for MTM Products)
Pitch	0.039” (1.00mm)

Table 2: MTM Edge Connector Specifications

Mechanical

Dimensions are shown in mm. 3D CAD models are available through the MTM-DEV-1 product page Downloads section and from: https://a360.co/31rZT7R

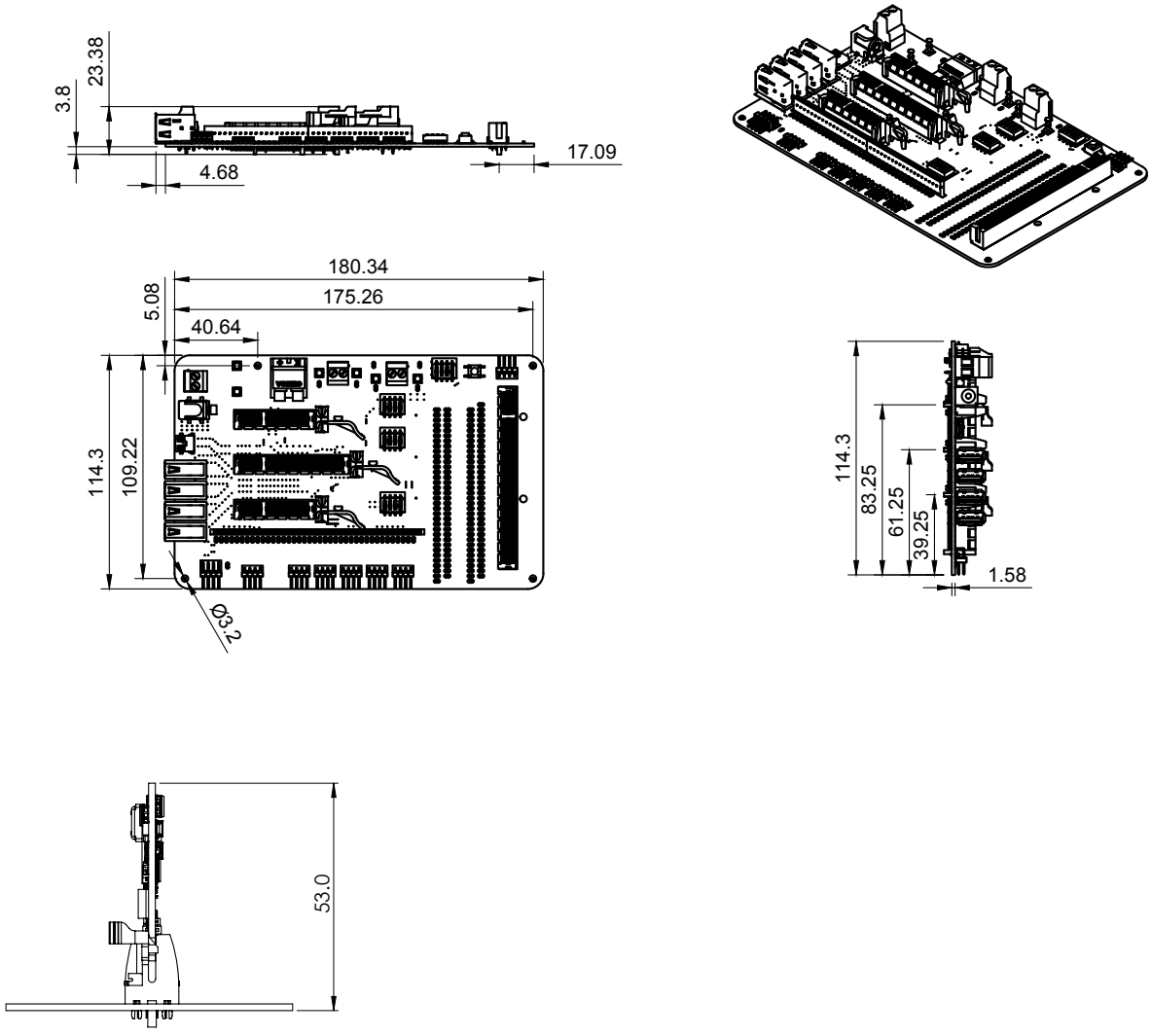

Figure 4: MTM-DEV-1 Mechanical

Module Address Hardware Offset Configuration

A hardware offset is one of two ways to modify the module's address on the BrainStem network. Using hardware offset pins is useful when more than one of the same type of module is installed on a single BrainStem network. Applying a different hardware offset to each module of the same type in one network allows for all the modules to seamlessly and automatically configure the network for inter-module communication. Further, modules can be simply swapped in and out of the network without needing to pre-configure a module's address before being added to a network. Finally, when a system has more than one of the same type of module in a network, the module address hardware offset can be used to determine the module's physical location and thus its interconnection and intended function. For detailed information on BrainStem networking see the BrainStem Reference**Error! Bookmark not defined.**.

Each hardware offset pin can be left floating or pulled to ground with a 1kΩ resistor or smaller (pin may be directly shorted to ground). Pin states are only read when the module boots, either from a power cycle, hardware reset, or software reset. The hardware offset pins are treated as a binary number which is multiplied by 2 and added the to the module's base address. The hardware offset calculation is detailed in the following table.

HW Offset Pin				Address Offset	Module Base Address	Final Module Address
3	2	1	0			
NC	NC	NC	NC	0	4	4
NC	NC	NC	1	2	4	6
NC	NC	1	NC	4	4	8
NC	1	NC	NC	8	4	12
1	NC	NC	NC	16	4	20
1	NC	NC	1	2+16	4	22

Table 3: Module address hardware offset examples

Document Revision History

All major documentation changes will be marked with a dated revision code

Revision	Date	Engineer	Description
1.0	July, 2020	ACRO	Initial Release